ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

Design of CMPFFE in current mode signalling for high performance and low power

Dr.J.Jebastine[1*], Francis Mary.T[2]
[1] ECE Department, Jeppiaar Engineering College, Chennai, India
[2]VLSI Design, Jeppiaar Engineering College, Chennai, India
***Corresponding author: E-Mail: enochjeba@gmail.com**

ABSTRACT

Low power is the major theme for electronics industry. An enormous portion of the on chip power is used by clock distribution network and flip-flops is made by clock system. The low power has caused a significant pattern shift where performance and area is main consideration for power dissipation. The substantial users of this power clock distribution networks (CDNs), global buses and synchronous signals. A new paradigm for clock distribution uses current rather than voltage to reduce power. This clock distribution network has been distributed to the one to many networks. One-to-one signals has been used in Current-mode (CM) signaling, this is the first manipulation in a one-to-multiple clock distribution network. To overcome this, we proposed a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using 180 nm CMOS technology. The CMPFFE also eliminates the need for complex CM receiver (Rx) circuitry and/or local VM buffers is used in conventional CM signaling schemes. To reduce the clock loads from the signal transmission circuits positive edge triggered signal is used. The design is carried out in Tanner EDA tool and the simulation results are based on 180nm technology for low power dissipation based flip-flop.

KEY WORDS: CMPFFE, Clock Distribution Network, Current mode.

1. INTRODUCTION

Digital systems are highly complex at their most detailed level. Convenient electronic devices require long battery lifetimes which can only be acquired by exploiting low-power components. They may consist of millions of elements i.e., transistors or logic gates whereas packaging and cooling only have a limited ability to remove the excess heat. Flip-flops (FFs) are the fundamental storage elements utilized extensively in all kinds of digital designs. In certain, digital designs now-a-days frequently validate intensive pipelining techniques and utilize many Flip-flop such as shift register, register file and first in- first out. Portable electronic devices need extended battery lifetimes only be acquired by utilizing low-power modules. Low-power design has become quite critical in synchronous system-on-chips (SOCs) and application specific integrated circuits (ASICs) because interconnect in technologies is utilizing an enlarged significant amount of power. The circuit power can be significantly decreased by reducing the clock power dissipation. The power delay is mainly due to the clock delays. It is estimated that the power consumption of the clock system, which composed of storage elements and clock distribution network. Flip-flops can change their content only either at the falling or raising edge of the activate signal. This enable signal is usually the clock signal. Later the rising or falling edge of the clock, the flip-flop content remains constant even. The S-R, J-K and D inputs are synchronous inputs because data on these inputs are fetched to the flip-flop's output on the triggering edge of the clock pulse. On the other, the direct clear (CLR) and set (SET) inputs are asynchronous inputs that modify the state of the flip-flop independent of the clock. Conventionally, the static power influence dynamic power consumption in a Current mode signaling scheme. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect.

2. METHODS AND MATERIALS

Current-Mode Pulsed Flip-Flop with Enable (CMPFFE): Current mode scheme is highly integrated into the Flip-flops that straightly obtain the CM signal to decrease overall power consumption and silicon area. Fig.1 show the circuit data of the existing current-mode pulsed DFF with enable (CMPFFE). It is identical to former CMPFF, but uses an active low enable signal. The CMPFFE uses an input current-comparator (CC) phase, a register phase and a static storage cell. The Current-comparator stage differentiate the input pushpull current with a reference current and conditionally amplifies the clock to full-swing voltage pulse that will triggers the data to latch at the register stage. The feedback pulsed Flip-flop is in distinct to the prior CM schemes which utilized expensive Rx circuits and buffers to drive the final FFs. The CMPFFE in Fig 1 is only intuitive to unidirectional push current which allows the positive edge trigger operation of the flip-flop. In order to efficiently receive an input pulse current, a CM Rx requires a low input impedance (Z_{in}). A small signal analysis at the input of the proposed CMPFFE ensures the low Z_{in} according to

$$Zin = 1/g_{m1} + g_{m2}$$

where g_{m1} and g_{m2} are the trans conductance of transistor M1 and M2, respectively. The input impedance of the proposed CM FF is also same to the former reported variation-tolerant CM signaling Rx.

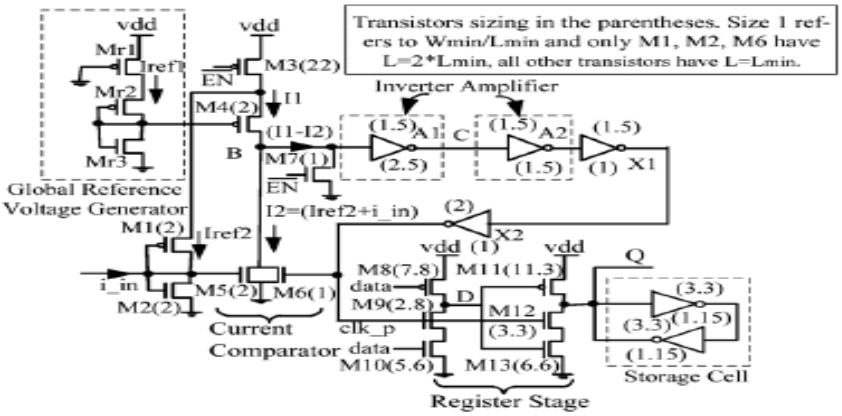

Figure.1.The existing CMPFFE uses current-comparator and feedback connection to initiate a voltage pulse that will triggers a register stage to store data in the storage cell.

Proposed Pulse Triggered Flip-Flop with CMPFFE: The existing is overcome by reduce clock loads, power and delay by giving pulse triggered flip-flop as clock signal. By using this method the current leakage is greatly reduced compared to conventional and existing design. Thus the proposed techniques are designed using CMPFFE with pulse triggered clock as shown in fig.2. Hence the design with reduced power consumption and delay is employed in application such as counters. The proposed method is similar as same as existing design but power consumption is greatly reduced in this method. In this method, pulse triggered clock controls CMPFFE. This method greatly reduce clock loads as well as power dissipation.

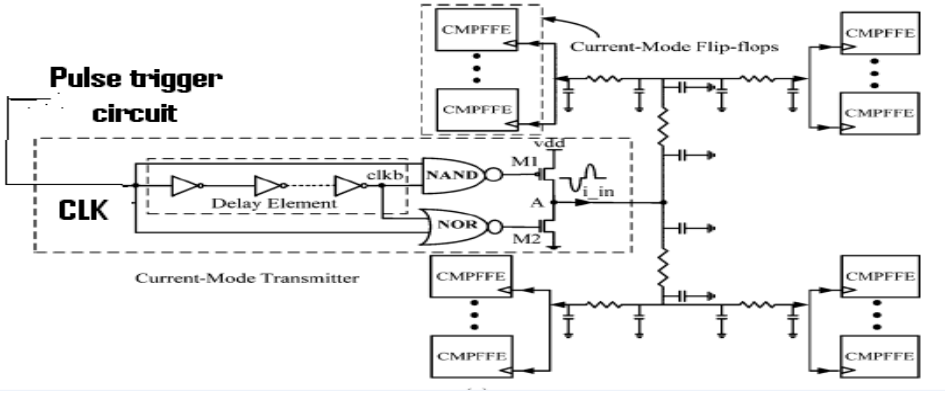

Figure.2.Proposed pulse triggered flip-flop with CMPFFE Circuit

3. RESULTS AND DISCUSSIONS

Pulse Trigger Output: Using of pulse trigger will greatly reduce the clock loads as shown in fig.3.In that diagram compared the normal clock pulse and positive edge triggered

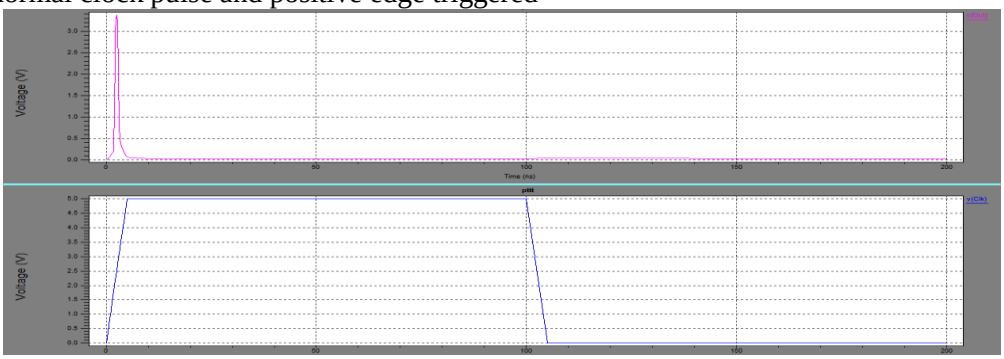

Figure.3.Comparison of normal and pulse triggered clock

CM CDN Analysis: In a VM CDN, the dynamic switching power of interconnect and clock load capacitances along with clock buffers dominate the power consumption. In a CM CDN, the power due to small fluctuations in and the Tx power contribute, but the static power of the CMPFFE dominates. In both cases, the number of sinks and chip dimensions increase the total power consumption. We use the same H-tree model in both the CM and VM CDN, but buffers drive the VM CDN instead of the CM Tx circuit. The VM buffered network is optimized for an output clock signal with less than 20 ps slew from 2–5 GHz. Since, the proposed CM FF is pulsed by nature, the VM CDN considers several pulsed FFs (Tra. PFF, CPEFF, DDPFF) and also considers the MS DFF as reference.

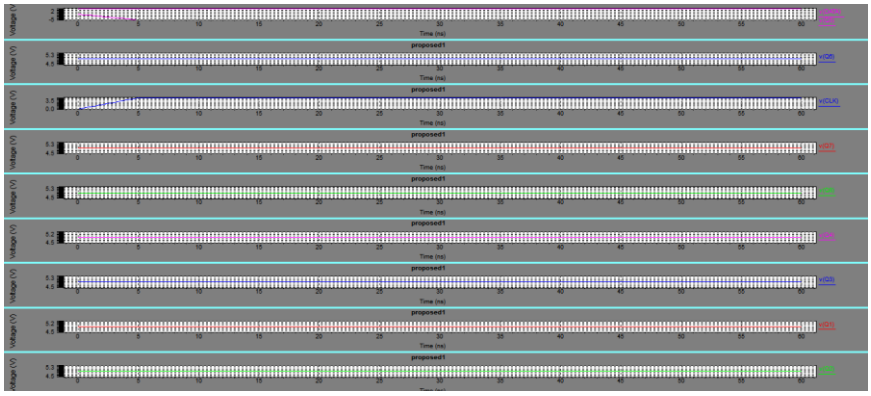

Figure.4.Proposed output waveform

Comparison Of Power Consumption In Existing And Proposed Design: We implemented our proposed CMPFFE using pulse triggered clock, a traditional VM master-slave DFF (MS DFF), a traditional VM pulsed FF (Tra.PFF), a high-performance conditional pulse-enhancement FF (CPEFF) and a recently reported low-power dual dynamic node pulsed hybrid FF (DDPFF). Total system power consumption of a CDN includes the CDN interconnect, buffer power and the FF power consumption.

Table.1. Comparison results for existing and proposed method

Types of flip-flop in existing and proposed	Power consumption Watts	Power consumption(w) at Temperature(degree)		
		20	40	60
CMPFFE	7.114856e-003	7.189995e-003	7.10881e-003	7.1208e-003
CMPFFE with pulse triggered	4.215818e-003	4.208248e-003	4.212230e-003	4.244438e-003

4. CONCLUSION

Hence, the proposed Technique greatly reduces the power consumption and clock loads by using pulse triggered clocked with CMPFFE. The proposed technique is overcome existing system by using positive edge trigger signal is transmitted. This technique results high performance with reduced power. Here the simulations are done using TANNER EDA tool under 180nm technology in order to provide accurate comparison with previous designs. The analysis of the proposed technique also takes various parameters like Power and Delay under consideration. Power is compared for existing and proposed techniques.

REFERENCES

Absel K, Manuel L and Kavitha R, Low-power dual dynamic node pulsed hybrid flip-flop featuring efficient embedded logic, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 21(9), 2013, 1693–1704.

Dave M, Jain M, Baghini S and Sharma D, A variation tolerant current-mode signaling scheme for on-chip interconnects, IEEE Trans, Very Large Scale Integr. (VLSI) Syst, 99, 2012, 1–12.

Kancharapu N.K, Dave M, Masimukkula V, Baghini M.S and Sharma D.K, A low-power low-skew current-mode clock distribution network in 90 nm CMOS technology, in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), 2011, 132–137.

Kim L and Kang S, A low-swing clock double edge-triggered flip-flop, IEEE J. Solid-State Circuits, 37(5), 2002, 648–652.

Narasimhan, Divekar S, Elakkumanan P and Sridhar R, A low power current-mode clock distribution scheme for multi-GHz NoCbased SoCs, in Proc. 18th Int. Conf. VLSI Design, 2005, 130–135.

Nikola Nedovic, Member, IEEE, and Vojin Oklobdzija G, Fellow, IEEE, Dual-Edge Triggered Storage Elements and Clocking Strategy for Low-Power Systems, IEEE transactions on very large scale integration(VLSI) systems, 13(5), 2005.

Peiyi Zhao, Jason McNeely, Weidong Kuang, Nan Wang, and Zhongfeng Wang, Design of Sequential Elements for Low Power Clocking System', IEEE transactions on very large scale integration (VLSI) systems, 19, 5, 2011.

Riadul Islam and Matthew R, Guthaus, Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop'IEEE transactions on circuits and systems—I, Regular papers, 62(4), 2015.

Islam R and Guthaus M, Current-mode clock distribution, in Proc. ISCAS, 2014, 1203–1206

Roy K, Mukhopadhyay S and Mahmoodi-Meimand H, Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits, Proc. IEEE, 91, 2, 2003, 305–327.

The CK, Hamada M, Fujita T, Hara H, Ikumi N and Oowaki Y,Conditional data mapping flip-flops for low-power and high-performance systems,' IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 14(12), 2006, 1379–1383.

Zhao P, McNeely J, Golconda P, Bayoumi MA, Kuang WD and Barcenas B, Low power clock branch sharing double-edge triggered flip-flop, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 15(3), 2007, 338–345.

Zhang H, Varghese G and Rabaey JM, Low swing on-chip signaling techniques, Effectiveness and robustness, IEEE Trans. Very Large Scale Integr. (VLSI) Syst, 8(3), 2000, 264–272.